REMARKS/ARGUMENTS

This application has been carefully reviewed in light of the Office Action dated December 31, 2003. Claims 1-4, 8-13 and 18-21 are pending in the application Claims 1, 10 and 18 are the independent claims. Claims 5-7 and 14-17 have been canceled without prejudice. It is believed that no new matter is involved in the amendments or arguments presented herein.

Reexamination and reconsideration of the amendment in the application are respectfully requested.

Art-Based Rejections

Claims 1, 2, 8-11 and 18-21 were rejected under 35 U.S.C. §103(a) over U.S. EP Patent Application Number 0,558,059 (Ishizaki) in view of U.S. Patent No. 6,229,515 (Itoh); Claims 3-4 and 12-13 were rejected under §103(a) over Ishizaki in view of Itoh and U.S. Patent No. 4,393,380 (Hosokawa). Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the arguments presented below.

The Ishizaki Reference

Ishizaki concerns a liquid crystal display including a liquid crystal sealed between a pair of substrates (*See, Ishizaki, abstract; Col. 3, lines 1-3*). According to Ishizaki the opposite electrodes are inverted and driven by the potential controlling device on the same substrate as the opposite electrodes (*See, Ishikazi, abstract; Col. 3, lines 17-30*).

The Itoh Reference

The ancillary Itoh reference a liquid crystal display device having selection switching elements. (See, Itoh, abstract; Col. 1, lines 5-7).

The Hosokawa Reference

The ancillary Hosokawa reference is directed to a matrix liquid crystal display circuit (*See, Hosokawa, abstract*). Hosokawa teaches the use of a common driver with a shift register for performing a memory function (*See, Hosokawa, Col. 7 line 35 to Col. 98, line 8*).

The Claims are Patentable Over the Cited References

The present invention is generally directed to a liquid crystal device and a method of driving same. As defined by independent Claim 1, a liquid crystal device includes M rows of scanning lines, wherein M is an integer equal to or greater than 2, and N columns of data lines, wherein N is an integer equal to or greater than 2. M X N number of switching element are respectively connected to one of the M rows of scanning lines and one of the N columns of data lines. M X N number of pixel electrodes are respectively connected to one of the M X N number of switching element. M rows of opposite electrodes are arranged oppositely to respective rows of the M X N number of pixel electrodes through a liquid crystal layer. A scanning line driving circuit configured to supply a scanning signal includes a scanning period for selecting at least one of the M rows of scanning lines to the M rows of scanning lines in each of a plurality of subfields defined by dividing one field. A signal control circuit is configured to convert a data signal to a binary signal in each of the subfields. A data line driving circuit is configured to supply a binary voltage to the N columns of data lines based on the binary signal from the signal control circuit. A polarity inverting circuit is configured to invert a polarity of a voltage applied to the liquid crystal layer by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in each of the subfields.

The cited references fail to disclose or suggest the above features of the present invention. In particular, the cited references fail to teach or suggest, for example, "a polarity inverting circuit configured to invert a polarity of a voltage applied to the liquid crystal layer by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in each of the subfields," as required by independent Claim 1.

Ishizaki concerns a liquid crystal display including a liquid crystal sealed between a pair of substrates (*See, Ishikazi, abstract; Col. 3, lines 1-3*). Ishizaki teaches that the opposite electrodes are inverted and driven by the potential controlling device on the same substrate as the opposite electrodes (*See, Ishikazi, abstract; Col. 3, lines 17-30*). According to Ishizaki, the potentials of the opposite electrode sections are inverted per frame or by line (*See, Ishizaki, Col. 5, line 30 to Col. 6, line 2*). In contrast, amended independent Claim 1 requires "a polarity inverting circuit configured to invert a polarity of a voltage applied to the liquid crystal layer by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in each of the subfields." This results in a more efficient operation and less power consumption for the present invention compared to that of the prior art. (*See application, page 29, lines 11-15.*)

Moreover, Ishizaki fails to disclose or suggest "convert a data signal to a binary signal in each of the subfields," as required by independent Claim 1.

The ancillary Itoh and Hosokawa references fail to remedy the above deficiencies of Ishizaki. Since the applied art of record fails to disclose, teach or suggest the above features recited in amended independent Claim 1, it cannot be said to either anticipate or render obvious the invention which is the subject matter of that claim.

The Office Action concedes that none of the cited references teach or suggest the above combination of features of the present invention, but nonetheless observes that the above combination "would have been obvious" to one of ordinary skill in the art. Applicants respectfully traverse this rejection.

Under MPEP §2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." Moreover, "the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure." Id. (citing In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

As MPEP §2143.01 makes clear, "***the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.***" Id. (citing In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)). It is respectfully suggested that none of the cited references suggest the combination of the above references. Moreover, none of the cited references contain a suggestion as to a reasonable expectation of success of any such combination.

Applicant respectfully submits that the finding of obviousness in this case is based on nothing more than the invention of the present application, and is thus improper. Should the examiner persist in maintaining this ground of rejection, Applicants respectfully request that the Examiner provide the Applicants with an affidavit for the purpose of appeal

Accordingly, independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested.

Applicant submits that amended independent claim 10 is also patentable over the applied references for at least the same reasons as those discussed above in connection with amended independent Claim 1.

Similarly, amended independent claim 18 is also patentable over the applied references for at least the same reasons as those discussed above in connection with amended independent 1. In addition, Ishizaki does not teach or suggest "supplying a binary voltage to a plurality of pixel electrodes based on the binary signal from the signal control circuit by data line driving circuit through N columns of data lines and a plurality of switching elements connected to the at least one selected scanning line," as required by independent Claim 1.

The remaining claims depend either directly or indirectly from amended independent Claims 1, 10 and 18, and recite additional features of the invention which are neither disclosed nor fairly suggested by the applied references and are therefore also believed to be in condition for allowance.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: April 30, 2004

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FIG. 10A
(Prior Art)

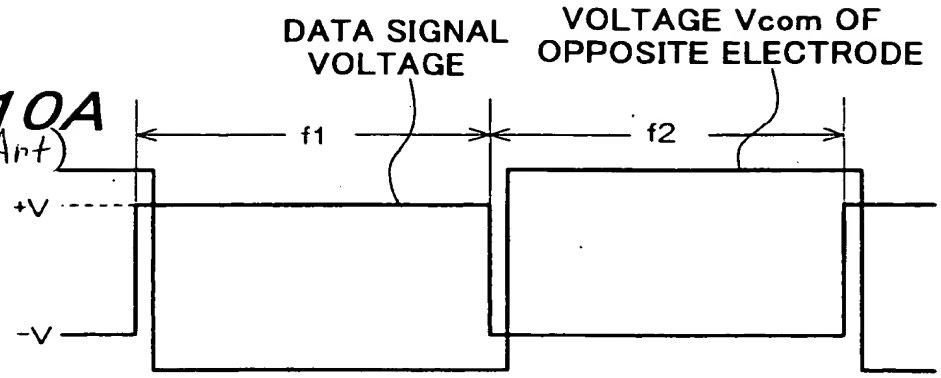


FIG. 10B
(Prior Art)

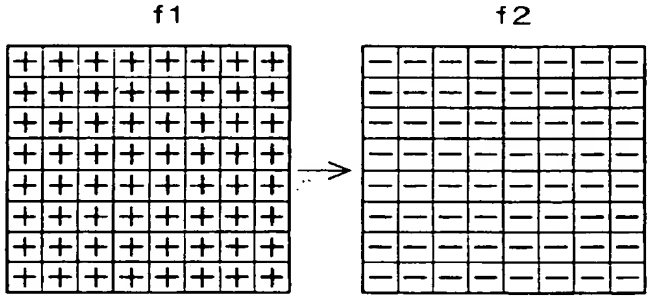


FIG. 10C
(Prior Art)

	f1					f2				
SELECTED PERIOD	H1	H2	H3	...	H240	H1	H2	H3	...	H240
SCANNING LINE 1			+5V					-5V		
SCANNING LINE 2	-4.9V		+5V			+4.9V		-5V		
SCANNING LINE 3	-4.9V			+5V		+4.9V			-5V	
⋮	⋮					⋮				
SCANNING LINE 240	-4.9V				+5V	+4.9V				-5V

FIG. 11A
(Prior Art)

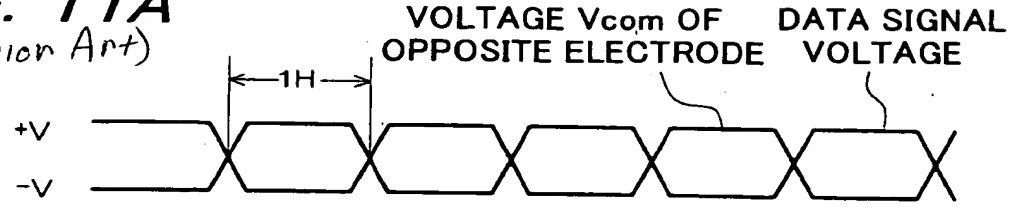


FIG. 11B
(Prior Art)

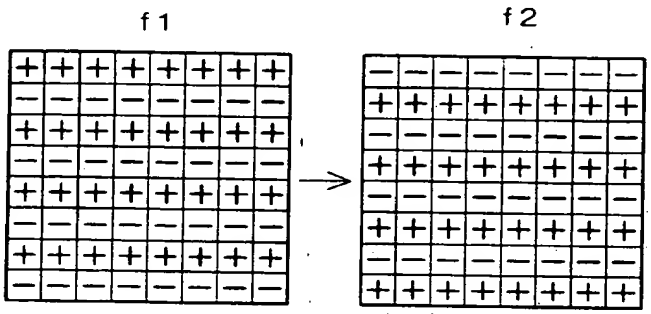
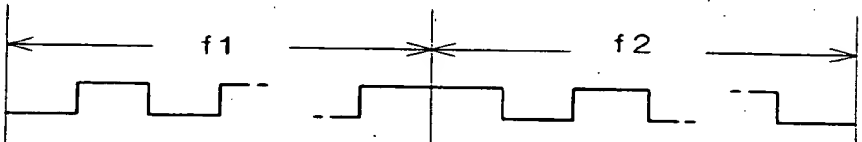


FIG. 11C
(Prior Art)



SELECTED PERIOD	H1	H2	H3	...	H240	H1	H2	H3	...	H240
SCANNING LINE 1	+5V	+4.9V	+5V	...	+4.9V	-5V	-4.9V	-5V		-4.9V
SCANNING LINE 2	+5V	-5V	-4.9V	...	-5V	-5V	+5V	+4.9V		+5V
SCANNING LINE 3	-4.9V	-5V	+5V	...	+4.9V	+4.9V	+5V	-5V		-4.9V
⋮			⋮					⋮		
SCANNING LINE 240	+5V	+4.9V	+5V	...	-5V	-5V	-4.9V	-5V		+5V